Application No.: 09/991,142 Docket No.: 21806-00134-US

REMARKS

Claims 1-10, 12-14 and 20-22 are presently pending in the application. Favorable reconsideration is requested.

Withdrawal of the rejection of claims 13, 14, 20 and 22 under 35 U.S.C. § 112 is requested. Claim 13 has been amended to more clearly claim the subject matter which was described in the specification (particularly on page 10, second full paragraph thereof).

Claim 20 has been amended to also more clearly claim the subject matter described in the specification.

Withdrawal of the objection to claim 5 is requested in light of the foregoing amendment thereto.

Withdrawal of the rejection of claims 2 and 20 under 35 U.SC. § 112 is requested in light of the amendments of claims 3 and 20.

Withdrawal of the rejection of claims 1, 2, 7, 9, 12 and 21 under 35 U.S.C. § 102 as being anticipated by Yagi et al. (U.S. Pat. No. 4,038,680) is requested. The Yagi et al. device discloses transistors which are formed in an integrated circuit. FIG. 7J, referred to in the Office Action, shows two bipolar transistors side-by-side. The devices are constructed so that they have a high withstanding junction voltage, as well as a high current and frequency gain amplification factor h_{FE}.

The reference does not appear to show any subcollector structure which would, as provided for in accordance with rejected claim 1, have a lateral ballasting effect. It appears from reviewing the description of the disclosed transistors of FIG. 7J that no subcollectors are referred to, and there does not appear to be any sheet resistance characteristic which would improve lateral ballasting of the transistor.

Rejected claims 2, 7-9, 12 and 21 all refer to characteristics of the subcollector region which improve the ballasting during an ESD event. It is submitted that nowhere within the reference is there any such description of an equivalent structure.

Withdrawal of the rejection of claims 1, 2, 6, 9, 12 and 21 under 35 U.S.C. § 102(b) as being anticipated by Watanabe et al. (U.S. Pat. No. 4,258,379) is requested. The cited reference is directed to a semiconductor and IC device which includes a bipolar transistor as well as an I^2L device. The bipolar transistor is designed to have a higher breakdown voltage without compromising the manufacturing yield for the device.

In reviewing the reference, it does not appear to provide for any ballasting which would help protect the device during an ESD event. In fact, there is no indication that there is any ESD protection in reading through the specification. The present invention as exemplified by the rejected claims requires two transistor devices, wherein one of them has a subcollector which has a particular sheet resistance to provide lateral ballasting of the second subcollector during ESD protection. Without such structure, it is not seen how the claims can be anticipated by the reference.

Withdrawal of the rejection of claims 3-5 under 35 U.S.C. § 103 as being unpatentable over Watanabe et al. (U.S. Pat. No. 4,258,379) further in view of Yamaguchi (JP 63-288055) is requested. As noted in the Office Action, the primary reference to Watanabe et al. (U.S. Pat. No. 4,258,379) does not disclose the required subcollector structures nor does it suggest having such structures with the required implant doseage.

Turning now to the secondary reference to Yamaguchi (JP 63-288055), a transistor structure is shown having an improved current amplification factor (h_{FE}) and frequency characteristic. The shown structure includes a first buried layer and a second buried layer in contact with a base region of a multi-collector transistor. The device, at least in the English language abstract thereof, makes no reference to any ESD ballast resistor formed in a subcollector. The device appears to be directed to improving the current gain and frequency characteristics, and not with any type of ESD protection. Accordingly, it is not seen how it can

be combined with the primary reference to derive the structure of Applicants rejected claims 3 and 5, which have specific limitations relating to the subcollector of one transistor.

Withdrawal of the rejection of claim 10 under 35 U.S.C. § 103(a) as being unpatentable over Watanabe et al. (U.S. Pat. No. 4,258,379) further in view of Hèbert et al. (U.S. Pat. No. 6,365,447) is requested. The Hèbert et al. reference as well does not disclose any structure for providing ballasting, through a subcollector as required by the claims. Further, there does not appear to be any ESD protection suggested in the specification of Hèbert et al. (U.S. Pat. No. 6,365,447). The Hèbert et al. device is apparently directed only to fabricating complementary bipolar transistors which have a high-frequency and high-voltage application. The reference describes a bipolar device as well as a BiCMOS device on a common substrate.

Withdrawal of the rejection of claims 20 and 22 under 35 U.S.C. § 103 as being unpatentable over Watanabe et al. (U.S. Pat. No. 4,258,379) further in view of Washio et al. (U.S. Pat. No. 4,694,321) is requested. The secondary reference to Washio et al. also discloses an integrated injection logic (I^2L) device with a bipolar transistor. This reference as well does not appear to provide for any ballasting during an ESD event, as set forth in the rejected claims. Claims 20 and 21 depend from claim 1, and require that there be a second semiconductor device with a subcollector with a different doping concentration provides for ESD robustness of the first semiconductor device. The second I^2L device does not appear to include the ESD protection of the claimed device.

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In view of the foregoing, favorable reconsideration is believed to be in order.

Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 09-0456, under Order No. 21806-00134-US from which the undersigned is authorized to draw.

Dated: 1/7/05

Respectfully submitted,

By _____

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